REMARKS

Claims 35-67 remain pending. Applicants respectfully submit that the primary reference, newly cited by the Examiner, the *Lin* reference (U.S. Published Patent Application 2003/0122240), is not prior art. Because *Lin* is newly cited along with *Bhakta* (U.S. Patent No. 6,222,739) and is not prior art, Applicants further respectfully submit that they have not had a full and fair hearing. MPEP § 706.07. In the alternative, *Lin & Bhakta* do not teach or suggest each and every feature of independent claims 35 and 67, and do not teach or suggest a recess. Applicants, therefore, respectfully request withdrawal of the final office action and reconsideration of the present application.

Lin is not prior art

The subject matter of the present application was conceived of prior to the effective date of *Lin*, May 19, 2000. The attached declarations and exhibits show, under penalty of perjury, that the subject matter claimed in claims 35-67 was conceived of prior to May 19, 2000.

Exhibit A shows 2 pages of notes prepared by Michael Chabot while implementing certain manufacturing processes for making certain carrier designs and assemblies for Kenneth Kledzick that are the subject of the present patent application. This document was prepared prior to May 19, 2000. Exhibit B shows these same 2 pages with specific drawings circled for the Examiner's convenience. These drawings support the declarations of both Kenneth Kledzick and Michael Chabot that the subject matter of claims 35-67 in the present application was conceived of prior to May 19, 2000, and that Michael Chabot began implementing certain manufacturing process for making the designs shown in these exhibits. The declarations further attest that work on this material continued until the present patent application was filed.

For example, the circled portion on page 1 of Exhibit B shows the subject matter claimed in claim 35. The drawing shows a carrier with a ball grid array, two IC packages with ball-grid arrays attached to the top and the bottom of the carrier, and a ball-grid array on the carrier for connecting to a circuit board. It is the recollection of Kenneth Kledzick, as reflected in his declaration, that the carrier represented by this drawing also included an interface and mounting pad arrays for the IC package and that the carrier interface and the mounting pad arrays were conductively bonded. He also recalls, as reflected in his declaration provided with this response,

that the carrier included an interface between the carrier and connection pads on a circuit board to which it may be attached.

As shown by the Chabot and Kledzick declarations and the attached Exhibits, the subject matter of the present application was conceived of prior to the effective date of *Lin* and due diligence continued toward a reduction to practice until the present application was filled. Accordingly, *Lin* is not prior art to this application.

Full and Fair Hearing

Applicants also submit that rejecting the present claims with newly cited references, *Lin* and *Bhakta*, in a final office action did not provide the Applicants with a full and fair hearing. *See* MPEP § 706.07. The fact that *Lin* is not considered prior art places Applicants further without a full and fair hearing. Applicants have not resorted "to technical or other obvious subterfuges in order to keep the application pending." MPEP § 706.07. Furthermore, a final office action is not appropriate when the Examiner switches "from one set of references to another." MPEP § 706.07. Applicants, therefore, respectfully request withdrawal of the present final office action for full and fair consideration of these newly cited references, especially in light of the fact that *Lin* is not prior art as discussed above.

Bhakta & Lin do not Teach or Suggest each and every Feature of Claims 35-36, 39-40, 42-43, 45-46, 49-53, 54-58, 59-62 and 64-67

The Examiner has not shown how the combination of *Bhakta* and *Lin* teach or suggest each and every feature of independent claims 35 & 57. Specifically, the Examiner has not shown at least where the combination teaches or suggests connecting a carrier with a circuit board with BGAs. Claim 35 comprises at least the following two features 1) two IC chips connected to a carrier with connection elements and 2) a carrier connected to a circuit board with BGA connections. *Bhakta* on the other hand teaches 1) a plurality of IC chips connected to an auxiliary circuit board with a pin-grid array and 2) an auxiliary circuit board connected to a main circuit board with surface mount connectors. The Examiner claims that it would be obvious to use a BGA when a pin-grid array is taught, as in *Bhakta*. This characterization is incorrect. Applicants use BGA connectors to connect a carrier with a circuit board; *Bhakta* uses a pin-grid array to connect components to an auxiliary board. The Examiner applied the connection type disclosed in *Bhatka* to connect components to an auxiliary board to make an obviousness

argument for a connection type connecting a carrier with a circuit board. The Examiner, however, has not shown how this combination from the references cited teaches the elements of, at least, claims 35 & 57.

The surface mount connectors in *Bhakta* do not teach or suggest BGAs. Indeed, *Bhakta* teaches away from BGAs. The BGAs in claims 35 & 57 are "conductively bonded" to the circuit board; thus creating a mostly permanent connection between the two. The surface mount connections in Bhakta, on the other hand are described as "easily connected and disconnected." Col. 7 line 58. Thus, *Bhakta* teaches auxiliary boards that can be connected and disconnected while the claims' BGAs require a more permanent bond.

Furthermore, the Examiner discusses *Bhakta* in regard to Fig. 8 only and disregards Fig. 7, which shows differences from claims 35 & 57. Fig. 8 should not be analyzed without reference to Fig. 7, to which it refers. *Bhakta* refers to FIG. 8 as "an exploded cross-sectional view of the expansion module illustrated in FIG. 7." The specification also discusses these figures in relationship to each other, for example as follows: "Referring now to FIGS. 7 and 8" (col. 7 line 24) and "With further reference to FIGS. 7 and 8" (col. 8 line 50). Thus, to be accurate, any discussion of Fig. 8 must include reference to and in the context of Fig. 7. Fig. 7 shows surface mount connectors 166a & 166b. The surface mount connectors in Fig. 7 & 8 require a physical connector on both the auxiliary board and the circuit board, as shown, whereas BGA connectors only require a BGA on the carrier and a pad on the board. Also, surface mount connectors are removable whereas BGA connectors are conductively coupled. The surface mount connectors shown in Fig. 7 do not render BGA connectors obvious because BGAs are distinct from surface mount connectors. Therefore, *Bhakta* does not teach or suggest each and every feature of claims 35 & 57.

Lin also does not teach a carrier with BGAs. Rather, *Lin* shows a carrier with big solder balls (BSBs). The BGAs in these claims are not BSBs, rather the BGAs in these claims are, for example, standard BGAs. The carriers described by these claims implement BGAs, not BSBs.

Accordingly, Applicants respectfully request withdrawal of the rejection of independent claims 35 & 57 and the rejection of corresponding dependent claims 36, 39-40, 42-43, 45-46, 49-53, 54-56, 58, 59-62 and 64-67.

The Recess in Claims 38, 41, 49, 52, 53, 58, 59 and 66

Claims 38, 41, 49, 52, 53, 58, 59 and 66 discuss a carrier comprising a recess. The Examiner explains that reference 167 in Fig. 8 of *Bhakta* shows a recess. However, the specification notes that 167 is a chip, not a recess, which is mounted in an opening. An opening and a recess are not the same. A recess connotes, without defining the term, a hollow or enclosed space, whereas an opening is not a hollow enclosed space, but rather open on both ends. Thus, *Bhakta* does not teach or suggest a recess in a carrier.

Lin also does not teach a carrier comprising a recess. In these claims a carrier comprises a recess, whereas in *Lin* the big solder balls (BSBs) create a space beneath the carriers. In *Lin*, no carrier having a recess is disclosed. Rather, a space is created beneath the BSBs by the relative size of the BSBs. Neither, *Bhakta* nor *Lin* teach or suggest a carrier comprising a recess. Applicants respectfully request that the rejection of claims 38, 41, 49, 52, 52, 58, 59 and 66 should be withdrawn.

Rejection of Claims 37, 41 and 48

The Examiner rejects dependent claims 37, 41 and 48 as being unpatentable over *Bhakta* and *Lin* and further in view of *Shim* (U.S. Patent No. 6,683,377). Applicants have shown above that independent claim 35 is not obvious in view of *Bhakta* and *Lin* because these references do not teach or suggest each and every element of the claim; thus dependent claims 37, 41 and 48 are not obvious in light of *Bhakta* and *Lin*. *Shim* does not teach or suggest those features of the claims not taught or suggested by *Bhakta* and *Lin*. Furthermore, as discussed above *Lin* is not prior art and *Shim* and *Bhakta* alone do not render claims 37, 41 and 48 obvious. Thus, claims 37, 41 and 48 are not obvious in light of *Bhakta*, *Lin* and *Shim*. Applicants respectfully requests withdrawal of the rejection of claims 37, 41 and 48.

Rejection of Claim 38

The Examiner also rejects claim 38 as being obvious over *Bhakta* and *Lin* as applied to independent claim 35 and further in view of *Ishii* (U.S. Patent No. 5,744,862). Applicants have shown above that *Bhakta* and *Lin* do not disclose all the claim features of dependent claim 38, in part, because *Lin* is not prior art. *Ishii* does teach or suggest those claim features not taught by *Bhakta* and *Lin*. Therefore, the combination of *Lin, Bhakta* and *Ishii* do not render dependent claim 38 obvious.

Rejection of Claims 44 and 63

Finally, the Examiner rejects claims 44 and 63 as being unpatentable over *Bhakta* and *Lin* and further in view of *Herrell* (U.S. Patent No. 6,828,666). Applicants have shown above that *Bhakta* and *Lin* do not disclose all the claim features of dependent claims 44 and 63, in part, because *Lin* is not prior art. *Herrell* does teach or suggest those claim features not taught by *Bhakta* and *Lin*. Therefore, the combination of *Lin, Bhakta* and *Herrell* do not render dependent claims 44 and 63 obvious.

CONCLUSION

Claims 35-67 are pending and believed allowable. Applicants have shown that the *Lin* reference is not prior art and in the alternative, *Lin* in combination with *Bhakta* does not render the present claims obvious. Also, Applicants have requested a full hearing in light of the newly cited references, one of which is not prior art. Applicants have also respectfully requested reconsideration of the present application in regard to the above arguments.

A Petition for Extension of Time is submitted concurrently with this amendment. The extensions of time fees are also submitted herewith. If there are any additional fees due in connection with the filing of this amendment, please charge the fees to the undersigned's deposit account, No. 50-3483.

If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

Respectfully submitted,

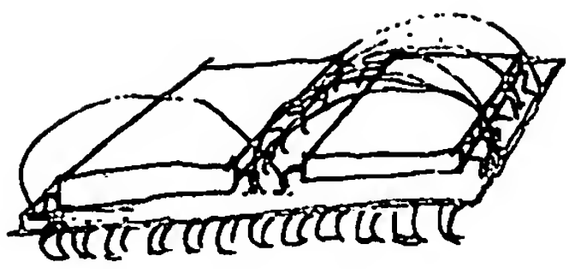
16 February 2006

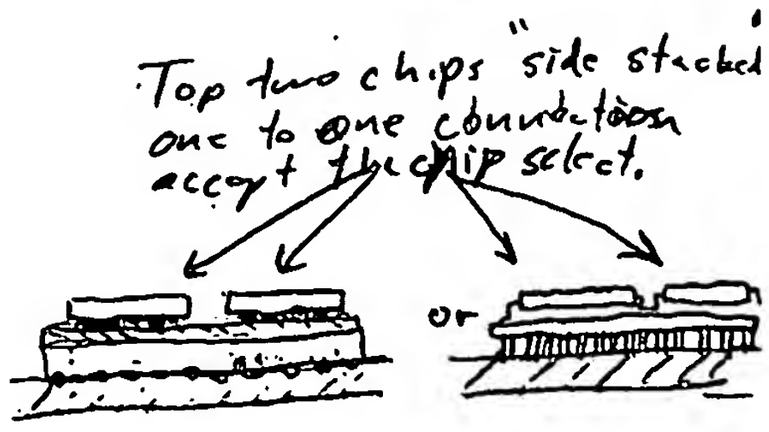
Jeff E. Schwartz
Reg. No. 39,019

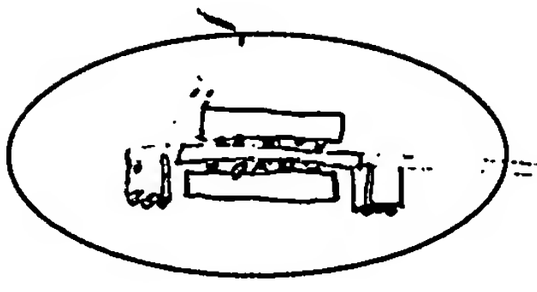
Schwartz Sung & Webster
300 Massachusetts Avenue, NW, Suite 1101
Washington, DC 20006
Telephone: 202.289.6291
Facsimile: 866.435.138

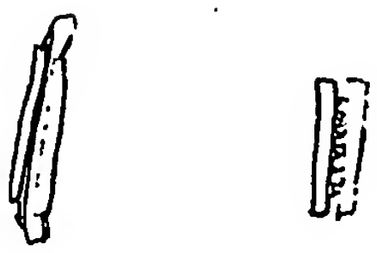
Legacy Electronics, Inc.

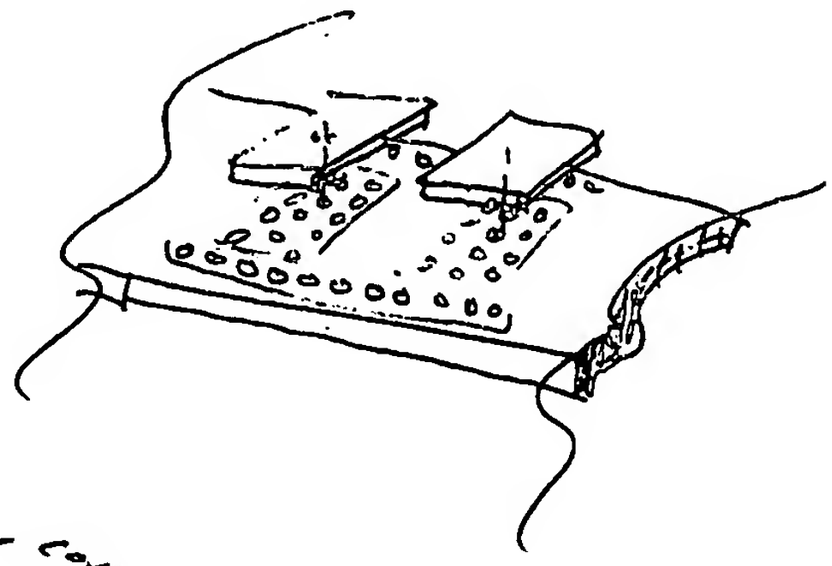
[redacted]

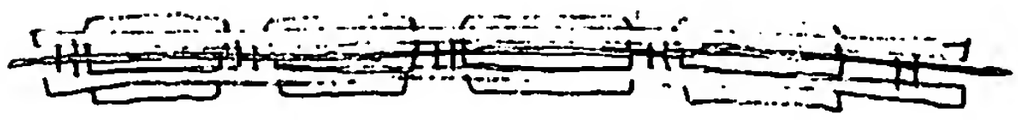


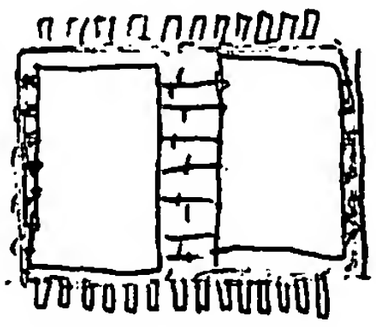


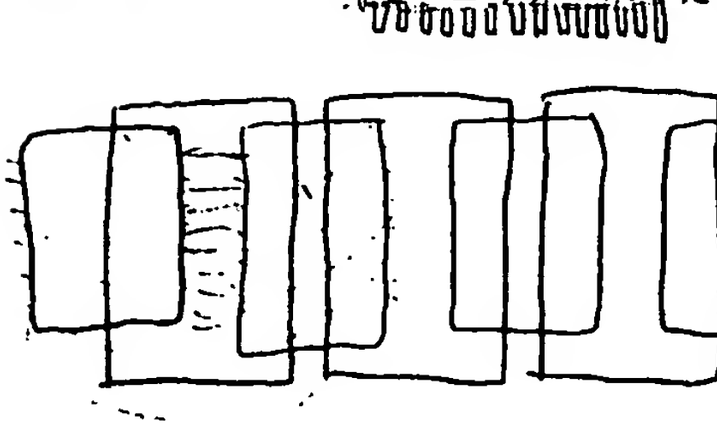


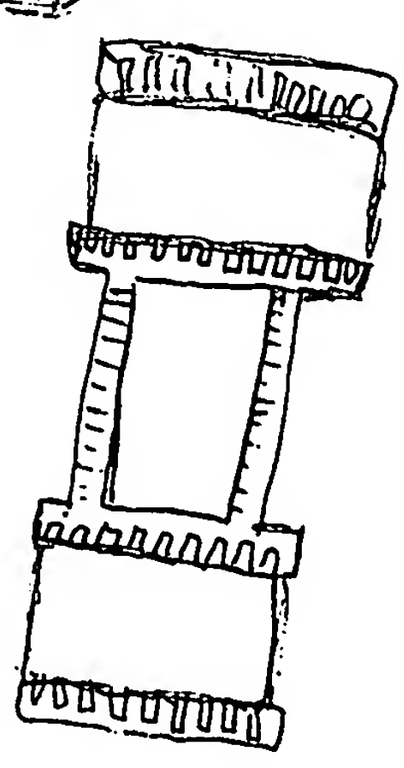


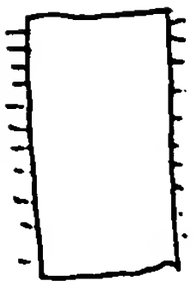


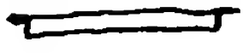








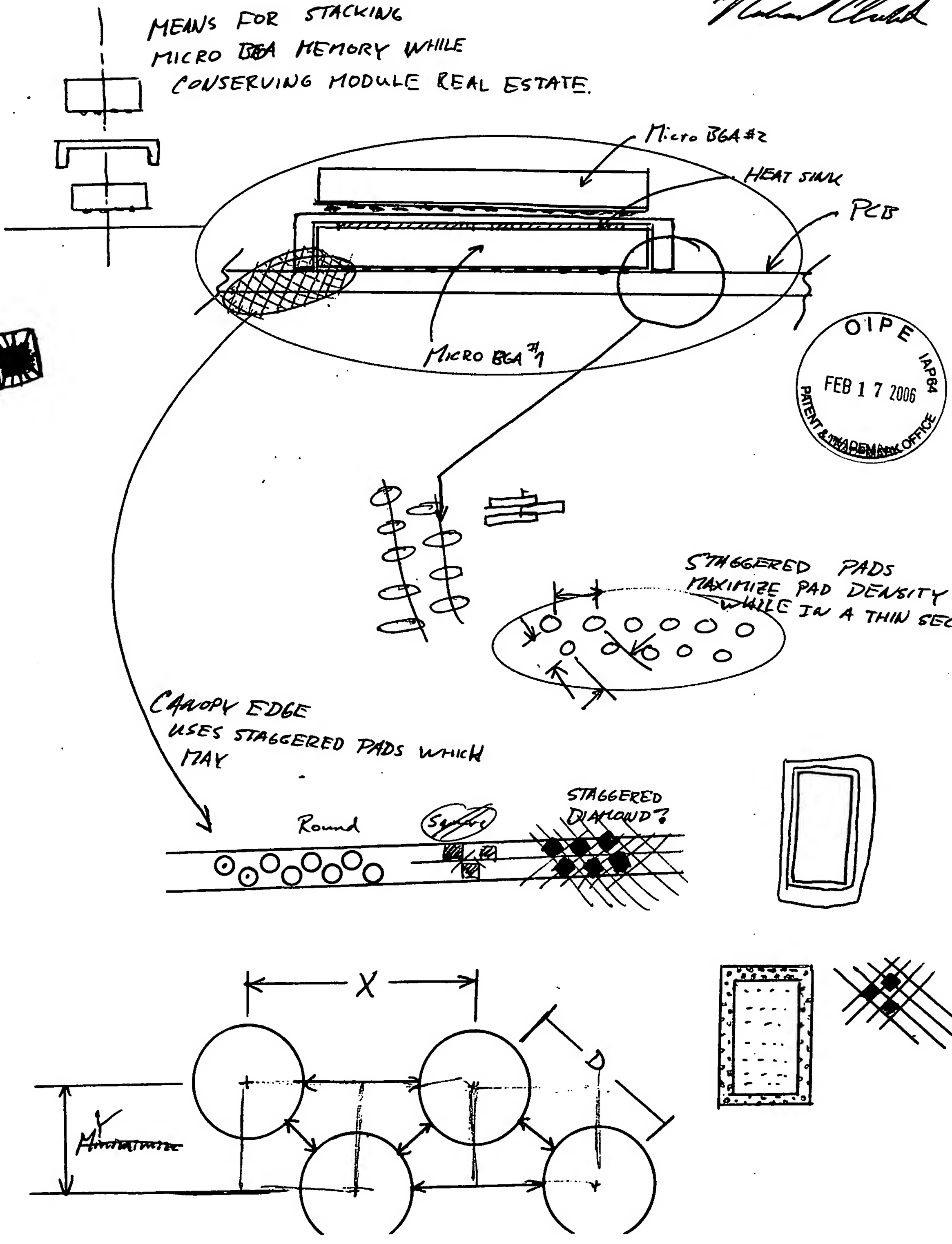




LEGACY ELECTRONICS, INC.

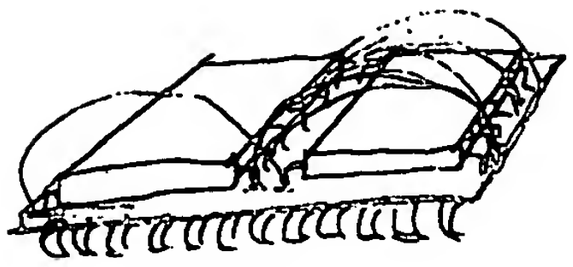
[redacted]

MEANS FOR STACKING
MICRO BGA MEMORY WHILE
CONSERVING MODULE REAL ESTATE.

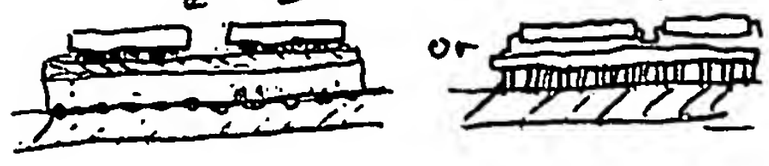


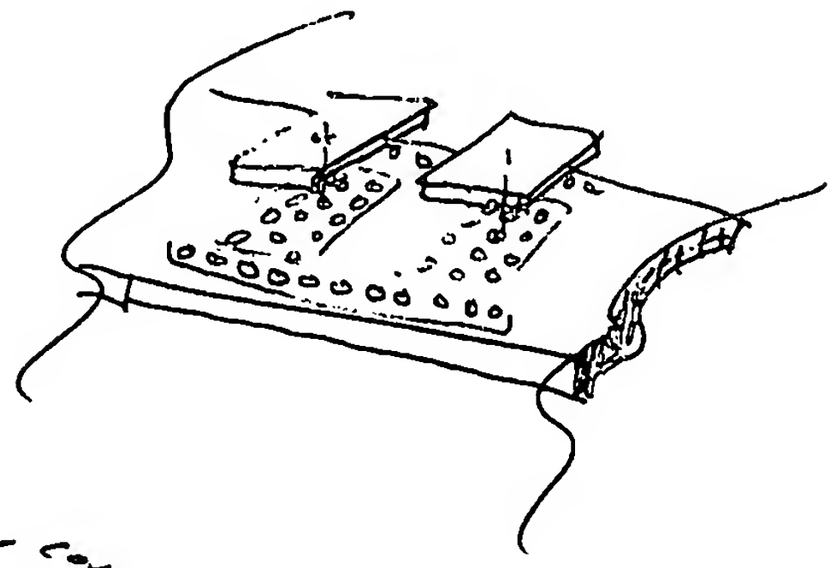
Legacy Electronics, Inc.

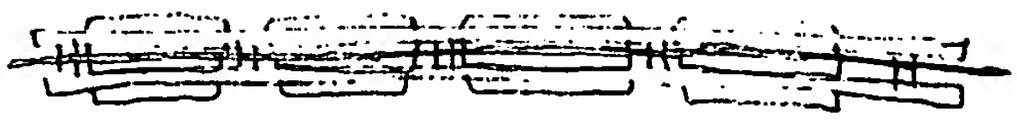
[redacted]



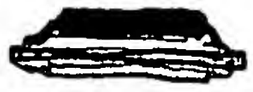
Top two chips "side stacked" one to one connection except the chip select.

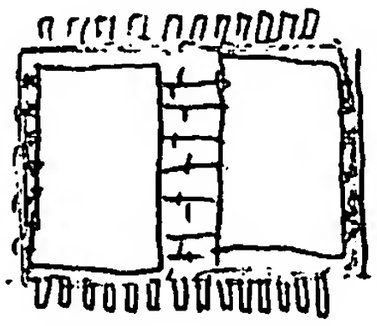


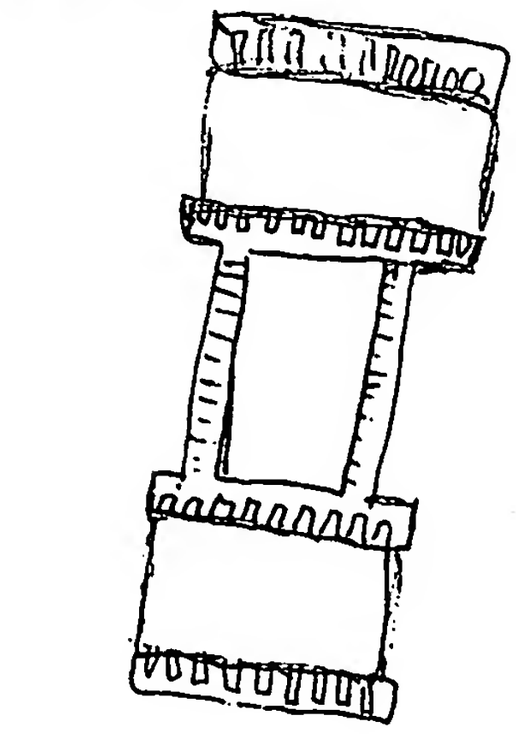


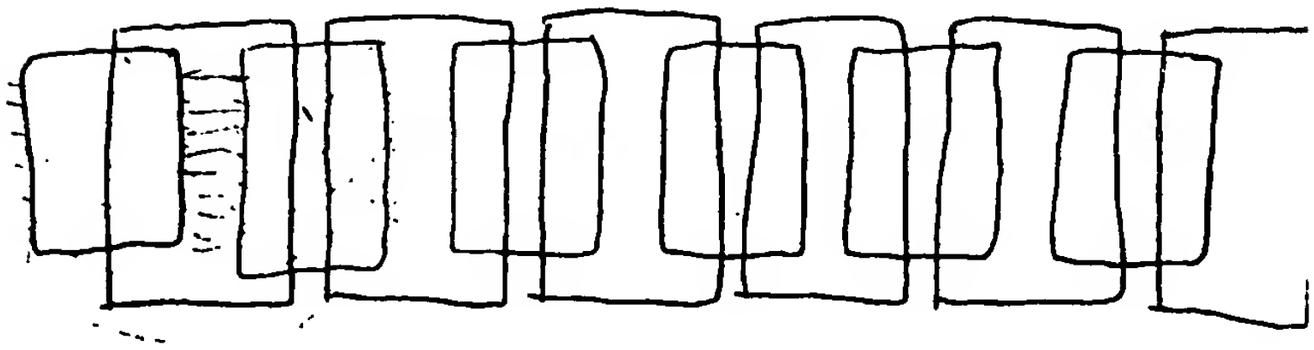


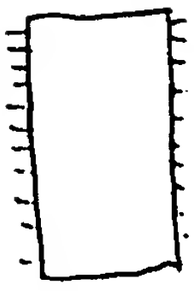
Common Ground Conductor

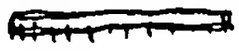


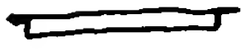








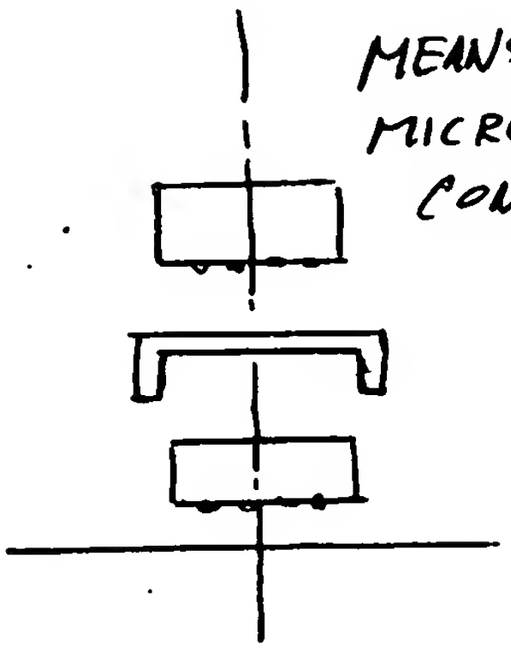


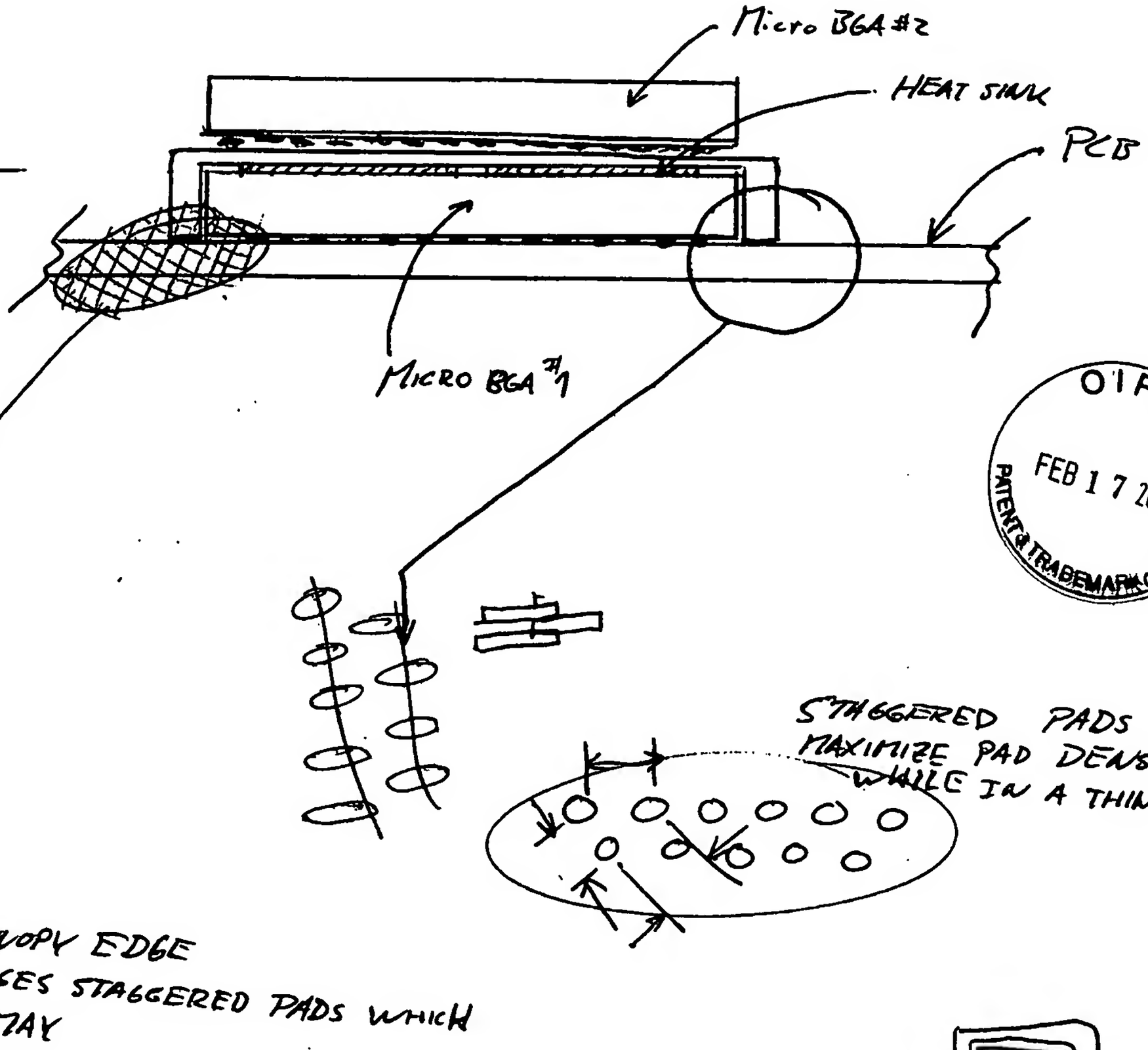


LEGACY ELECTRONICS, INC.

[redacted]

MEANS FOR STACKING
MICRO BGA MEMORY WHILE
CONSERVING MODULE REAL ESTATE.





STAGGERED PADS
MAXIMIZE PAD DENSITY
WHILE IN A THIN SECTION

CANOPY EDGE
USES STAGGERED PADS WHICH
MAY